AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 7, line 25, as follows:

It will be appreciated that in operation program instructions are fetched from memory addresses within a memory (not illustrated) and passed to the instruction prefetch buffer 14. When the program instructions reach the decode stage within the instruction prefetch buffer 14, the instruction decoders 12 decode these instructions and ~~generates~~ generate control signals which are applied to the processing logic within the processor core 3, and the coprocessor 22 as necessary, to control these other elements to execute the data processing operation(s) specified. The processor core 3 is operable in a first mode in which a first instruction set is being decoded and in a second mode in which a second instruction set is being decoded. One way of indicating which mode the processor core 3 is in is to use a flag value within one of the program status registers 18. Depending upon which instruction set is currently active, the instruction decoders 12 will interpret the instructions received in accordance with the currently active instruction set and its encoding. In accordance with the present technique, the two instruction sets supported share a common encoding for a common subset of instructions, including at least one class of instructions, such as all unconditional coprocessor instructions, thereby enabling ready reuse of the same physical hardware to implement those common processing operations. It will be appreciated that the storage order of the program instructions from the different instruction sets may vary, such as due to endianness differences, instruction word size differences and the like, but the common subset of instructions share an encoding once such storage order differences have been compensated for as will be discussed hereafter.